REMARKS

Applicant respectfully traverses and requests reconsideration. Furthermore, Applicant wishes to thank the Examiner for notice that Claims 1, 6-12 and 17-22 have been allowed.

Claims 7 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakatsuka et al., U.S. Patent No. 6,433,782 ("Nakatsuka") and Bogin et al., U.S. Patent No. 6,192,455 ("Bogin"). Applicant respectfully interprets the present Office Action's citations to Nakatsuka as teaching Applicant's Claim 7, Steps (b) and (d). (Page 3, lines 5-7).

Nakatsuka, among other differences, fails to teach a multiple translation process as claimed. As stated in the Applicant's previous two responses (filed 1/29/03 and 6/17/03), "the Nakatsuka reference appears to teach a conventional approach to address translation." Further, "Nakatsuka merely teaches the process in which an address is translated if a region determining unit determines that the corresponding data belongs in a particular region. Nakatsuka fails to teach or suggest a process in which a virtual address is first translated into an address [corresponding to Applicant's Step (a)] and then a determination is made as to whether the address corresponds to a translation memory space [corresponding to Applicant's Step (b)]." (Response filed 6/17/03, Page 5, lines 1-5; Col. 9, lines 12-22). Because Applicant's Step (b) is dependent upon Step (a) to the extent that "the address" of Step (b) was formed from a translated virtual address as indicated in Step (a), Nakatsuka fails to teach Applicant's Step (b).

Similarly, Nakatsuka is not directed at Step (d), a process dependent upon both Steps (a) and (b). Because Nakatsuka does not teach "an address," previously translated from a virtual address as claimed in Step (a), and further fails to teach the determination process of Applicant's Step (b), Nakatsuka necessarily fails to teach the translation of "the address" [of Step (a)] into

another address when "the address" corresponds to translation memory space. As a consequence, Applicant contends that Nakatsuka fails to teach Applicant's Step (d).

Moreover, Nakatsuka teaches away from Applicant's claimed invention as Nakatsuka appears to teach a single translation contingent upon a region-determining unit's determination that corresponding data belongs to a particular region. In contrast, Applicant discloses a process that includes up to two translations. Nakatsuka appears to teach away from Applicant's Claim 7.

To illustrate Nakatsuka's use of a process that includes up to one translation, Applicant respectfully directs the Examiner's attention to Col. 3, lines 15-35 and Figs. 3b-3d of the Nakatsuka reference. Specifically, this reference illustrates that an object of the Nakatsuka reference is to provide a data processing apparatus that can access, at high speeds, a memory where various kinds of data with different addresses are mixed and stored. To accomplish this end, Nakatsuka utilizes a memory unit having first data stored with a tile-type address in a graphics region (See Fig. 3c; Logical Address For Graphics Processor) and a second data stored with an array type-address in a program region (See Fig. 3b; Logical Address For Data Processor).

Applicant respectfully draws the Examiner's attention to Fig. 3d to illustrate the relationship between the physical address of the memory unit, the logical address of the graphic processor and the logical address of the data processor. The Nakatsuka reference instructs that "the graphics processor accesses the memory unit in accordance with an instruction from the data processor" (Col. 8, lines 50-52) and determines whether the required data is located in the graphics or program region via a region determining unit (Col. 8, lines 13-22). Because the physical addresses and graphic processor addresses directly correspond to the pixel data, picture processing is 'sped up' *as address translation between the memory unit and the graphic*

processor is not required. (Emphasis added). However, access from the data processor to pixel data is performed by converting the logical address of the data processor into the picture logical address or physical address (Col. 8, line 62 - Col. 9, line 7). As a result, only one translation *may* occur in the Nakatsuka reference. In contrast, Applicant's Claim 7 is directed at a process where up to two translations may take place. In other words, Applicant's Claim 7 requires a minimum of one translation [Step (a)] and a maximum of two translations [Steps (a) and (c)]; Nakatsuka only allows one translation upon a determination that certain events are fulfilled. Applicant contends that Nakatsuka teaches away from Applicant's claimed invention.

Contrary to the Office Action's assertion that Bogin teaches Steps (a), (c) and (e) of Applicant's Claim 7, Applicant respectfully contends that Bogin is directed at an apparatus and method for preventing access to a system management random access memory (SMRAM) space, *utilizing a single virtual to main memory address translation step.* As such, Bogin appears to also teach away from Applicant's claimed invention.

As Bogin discloses, requests to access system memory are forwarded to the host bridge (Element 130) by various devices. Configured with a destination address where a read or a write is to be directed, each request to access system memory is sent to an arbiter (Fig. 3, Element 310) of the host bridge. If the request's destination address needs no translation (and therefore does not correspond to a AGP request), then the arbiter of the host bridge forwards the access request and address to a cycle tracker. Otherwise, if the request requires a translation and therefore is directed to the AGP aperature memory (as illustrated by line element 320 of Fig. 3), then the arbiter forwards the request to an AGP translator for translation (Fig. 3, Element 308; Col. 5, lines 3-8).

As a result, it is clear that Bogin fails to teach Applicant's Step (a) of Claim 7. Step (a) requires, in all situations, that a virtual address be translated into an address. Bogin teaches that in the event of a non-AGP request, no address translation is needed and the request's destination address is forwarded to a cycle tracker by the arbiter (Col. 5, lines 3-5). Furthermore, Bogin fails to disclose Applicant's Step (c). Step (c) not only depends upon Step (a) but also requires that the *translated* address be stored in a translation look aside table when the address does not correspond to the translation memory space. (Emphasis added).

To the extent that the Bogin reference can be compared to Applicant's Step (c), Applicant notes that the event of a non-AGP request (Fig. 3, Element 322) as taught by Bogin is most comparable to Applicant's determination of when the (previously translated) address does not correspond to the translation memory space [Step (c)]. However, as stated above, Bogin fails to teach the translation step of Applicant's Step (a) and therefore also fails to teach Step (c). Furthermore, Applicant's Step (c) requires the caching of the previously translated address in a translation look aside table. In contrast, Bogin teaches that no translation look aside table is required in the event of a non-AGP request as the address is forwarded to a system memory via the cycle tracker and memory interface of Fig. 3 (Fig. 3, Elements 322, 305, 132; Col. 5, lines 3-5).

As a necessary consequence, Bogin appears to teach away from Applicant's Claim 7. No combination of Bogin or Nakatsuka teach the claimed steps of Applicant's Claim 7. Because Claim 18 corresponds to the module (or apparatus) claim of Applicant's Claim 7, both Claims 7 and 18 appear to be in proper condition for allowance.

Claims 8-11 and 19-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakatsuka, et al. and further in view of Hayes, et al., U.S. Patent No. 6,356,989. Applicant

respectfully notes that Claims 8-11 and 19-22 are depending claims of allowable parent Claims 7 and 18, respectively. As such, Applicant respectfully reasserts the relevant remarks made above with respect to Claims 7 and 18. Furthermore, Applicant submits that Claims 8-11 and 19-22 are allowable as written for the same or similar reasons. Applicant further submits that the depending claims are also allowable in light of the presence of novel and non-obvious elements contained therein that are not otherwise present in the parent claim.

Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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